REMARKS

The Final Office Action mailed November 24, 2004, has been received and reviewed. Claims 1 through 25 are currently pending in the application. Claims 1 through 25 stand rejected. Applicants propose to amend claims 1, 13, 17, 23 and 25, and respectfully request reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 112 Claim Rejections

Claims 1 through 5, and 13 through 24 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

The Office Action states:

> As per claim 1, 13, 17, and 23, Applicant sets forth in the claims that the "data corresponding to the memory command arrives at the DRAM, implying that the data does not travel through the FIFO. Applicant also sets forth "simultaneous reading and writing of the at least one of data and commands from the FIFO", indicating that the data travels through the FIFO. It is not clear from the amended claim language whether the data travels through the FIFO or not. For purposes of applying the prior art, the Examiner will assume that the data travels through the FIFO. (Office Action, p. 2).

Applicants respectfully disagree with the Examiner's position because as per MPEP standards on clarity and precision of claim language (see MPEP §2173.02), the content of the application disclosure clearly teaches and discloses that one of ordinary skill in the art know that memory devices are accessed by memory commands that may include addresses and data. Applicants respectfully submit that as to relative or variable terminology in claims, Applicants maintain the position that "the fact that claim language . . . may not be precise, does not automatically render the claim indefinite under 35 U.S.C. 112, second paragraph." *Seattle Box Co., v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 221 USPQ 568 (Fed. Cir. 1984). Further, "[a]cceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification." MPEP §2173.05(b). Applicants respectfully submit that the disclosure of the present application provides abundant

disclosure and teaching on whether or not the data passes through the FIFO. More specifically, from the disclosure of the above-referenced application:

FIG. 1 illustrates addresses and address pointers coupled to the FIFO;

FIG. 7 illustrates FIFO Buffers 66 coupled to address registers and counters while the Data Registers are separately coupled to the memory banks;

In the Summary of the Invention, "In particular use with a dynamic random access memory (DRAM) device, the FIFO buffer system stores address commands until corresponding data to be stored arrives at the DRAM. This frees up the DRAM pipelines for use with transferring data rather than storing address commands for the data." (Applicants' specification at paragraph [0011]).

Applicants' respectfully assert that "data" (e.g., memory command/address information) in a buffer is not the same as "data corresponding to the memory command" which correlates to the data being read or written through the execution of the memory command. Through the claiming terminology of the present application, Applicants have maintained a distinction between "memory commands" and "data corresponding to the at least one memory command."

Applicants respectfully submit that the specification and claims are clear that "memory commands" are temporarily stored in the FIFO "until at least one of the data corresponding to the at least one memory command arrives at the DRAM." Clearly, the memory commands, and any information associated therewith, are stored in the FIFO until the data arrives at the DRAM.

Applicants, therefore, respectfully request reconsideration of claims 1 through 5, and 13 through 24.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,487,049 to Hang

Claims 1 through 4, 6, and 17 through 25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hang (U.S. Patent No. 5,487,049). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Hang references does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of independent claims 1, 6, 17 and 23, and claims depending therefrom, because the Hang reference does not describe, either expressly or inherently, the identical inventions in as complete detail as are contained in the claims.

The Office Action alleges:

> As per claim 1, Hang teaches, with respect to figure 1, a DRAM 16, a DRAM controller for controlling the DRAM (see column 4, line 30), and a FIFO 10 associated with the DRAM (see column 2, lines 60-63). Hang further teaches at column 3, lines 63-67, that the data register 30 and address register 34 are two-port memories which can simultaneously write data to a storage location having an address specified by a write count value while reading data from a different storage location having an address specified by a read count value. The claimed "control logic" is represented, at the least, by write counter 22, read counter 26, and state machine 20, as shown in figure 1. The FIFO temporarily stores addresses until a full page worth of data is stored in the data register for transfer to the DRAM. Hang sets forth that the address register FIFO 34 which holds 8 column addresses previously stored associated with data that is to be stored in the data register 30 and DRAM 16. See column 3, lines 62-67, and column 4, lines 26-29. (Office Action, p. 3).

Applicants respectfully disagree that the Hang reference anticipates Applicants' invention as claimed in presently amended independent claims 1, 6, 17, 23 and 25, an exemplary amended independent claim 1 of which reads:

> 1. A dynamic random access memory device (DRAM), comprising:
> at least one memory bank;
> control logic associated with the at least one memory bank to control data corresponding to a memory command within the DRAM; and
> a FIFO associated with the control logic, the FIFO configured for temporarily storing at least one ~~a~~ memory command until at least one of the data corresponding to the at least one memory command arrives at the DRAM, the at least one memory command including an address within the at least one memory bank, the control logic further configured for simultaneous reading and writing from the FIFO, ***the***

> ***control logic further including a read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter.*** (Emphasis added.)

In contrast to the elements of the presently claimed invention of exemplary amended independent claim 1, nothing within the Hang reference discloses ***maintaining a previous read counter setting***, as uniquely taught by Applicants and claimed within the each of the amended independent claims. In the Office Action's Response to Arguments section, the Examiner states:

> With respect to Applicant's arguments concerning the rejection of claims 11-12 under 35 U.S.C. 103, Applicant argues that Hang does not teach or suggest "at least one pointer register configured to maintain a previous read counter setting of the at least one read counter". However, the Examiner maintains that Hang teaches that the read counter 26 is incremented upon a particular assertion of DRAMREQ (see column 4, lines 24-26) and therefore, ***prior to the read operation, the read counter register is configured to maintain the previous read counter setting***. (Office Action p. 11, emphasis added).

Applicants respectfully assert that ***any counter that, "prior to [an] . . . operation . . . is configured to maintain [a] . . . setting" is merely configured to maintain the current setting and NOT configured to maintain a previous setting***, as claimed by Applicants.

Clearly, the Hang reference discloses only maintaining a current setting and NOT a previous setting, as claimed by Applicants. Applicants further submit that each pending independent claim includes similar elements, namely:

> 6. A FIFO buffer system in a dynamic random access memory device (DRAM), comprising:
> a FIFO . . .;
> at least one write counter . . .; and
> at least one read counter associated with the FIFO, the at least one read counter comprising ***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter.***
>
> 8. An electronic system, comprising:
> a processor;
> at least one of an input device . . .; and
> a memory device . . . comprising:
> at least one FIFO . . .;
> at least one write counter . . .; and

at least one read counter associated with the at least one FIFO, the at least one read counter comprising ***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter.***

11. A semiconductor substrate including a FIFO buffer, comprising:
at least one FIFO;
at least one write counter . . .; and
at least one read counter associated with the at least one FIFO, the at least one read counter comprising ***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter.***

13. A semiconductor substrate including a DRAM, comprising:
at least one memory bank;
control logic . . .; and
a FIFO associated with the control logic, the FIFO configured for temporarily storing a memory command until data corresponding to the memory command arrives at the DRAM, the control logic further configured for simultaneous reading and writing of the at least one of data and commands from the FIFO, the control logic further including ***a read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter.***

17. A method of storing data in a DRAM, comprising:
providing a DRAM comprising at least one memory bank, control logic . . ., and a FIFO . . ., the control logic further including ***a read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter;***
receiving the memory bank address command at the control logic;
writing the memory bank address command to the FIFO;
receiving data corresponding to the memory bank address command at the control logic;
reading the memory bank address command from the FIFO; and
storing the data at a memory bank address indicated by the memory bank address command.

23. A method of buffering a data stream including a memory bank address command and data corresponding to the memory bank address command in an electronic device, the method comprising:
providing a FIFO buffer system . . .;
receiving the memory bank address command of the data stream at the FIFO buffer system;
storing the memory bank address command of the data stream in the first buffer of the FIFO;
adjusting the write counter to point at a second buffer in the series of FIFO buffers; and
maintaining the write counter pointing to at least one FIFO buffer, in the series of FIFO buffers, ahead of the first buffer at which the read counter is pointing and

maintaining a read counter pointing to at least one FIFO buffer associated with a previous read counter setting.

25. A method of operating a memory device, the method comprising:
receiving at least one memory bank address command;
temporarily storing . . .;
temporarily storing in the FIFO a second of the at least one memory bank address command;
receiving data corresponding to the first of the at least one memory bank address command;
storing in the FIFO the data . . .;
receiving data corresponding to the second of the at least one memory bank address command;
storing in the FIFO the data . . .; and
maintaining the write counter pointing to at least one FIFO buffer, in the series of FIFO buffers, ahead of the first buffer at which the read counter is pointing and ***maintaining a read counter pointing to at least one FIFO buffer associated with a previous read counter setting.***

(Emphasis added.)

Furthermore, Applicants' claims as amended, do not introduce additional elements that require further searching or otherwise as **such elements** are in part similar to those elements of unamended independent claims 6, 8 and 11 that **were previously examined**. Therefore, independent claims 1, 6, 17, 23 and 25, and claims 2-5, 7 , 18-22, and 24, depending therefrom, are not anticipate by the Hang reference under 35 U.S.C. § 102. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in View of U.S. Patent No. 5,699,530 to Rust et al.

Claims 5 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Rust et al. (U.S. Patent No. 5,699,530). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 5 and 7 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Regarding claim 5, which depends from amended independent claim 1, Applicants sustain the above-proffered arguments that Hang does not teach, disclose or motivate Applicants' invention as claimed in amended independent claim 1. The Office Action cites the Rust reference for disclosing linear feedback shift registers. However, regarding claim 5, Applicants submit that any proposed combination of the Hang reference and the Rust reference does not teach or suggest the claim limitations calling for "***the control logic further including a read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter***", as claimed by Applicants in amended independent claim 1 from which claim 5 depends. Therefore, Applicants respectfully request that the rejection to claim 5 be withdrawn.

Regarding claim 7, Applicants submit that any proposed combination of the Hang reference and the Rust reference does not teach or suggest the claim limitations calling for "***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter***", as claimed by Applicants in independent claim 6 from which claim 7 depends. Therefore, Applicants respectfully request that the rejection to claim 7 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in View of U.S. Patent No. 5,289,584 to Thome et al.

Claims 8 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Thome et al. (U.S. Patent No. 5,289,584). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 8 through 10 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Regarding independent claim 8, from which claims 9 and 10 depend, Applicants sustain the above-proffered arguments that Hang does not teach, disclose or motivate Applicants' invention as claimed. In contrast to the elements of the presently claimed invention of independent claim 8, nothing within the Hang reference discloses "***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter***", as uniquely taught by Applicants and claimed in independent claim 8.

The Office Action cites the Thome reference for "teach[ing] a system including a page mode DRAM and a FIFO 114 or 116 (figure 2), which includes a CPU 30, keyboard 80 ("input device"), monitor 64 ("output device") and a hard disk 98 ("storage device"). See figure 1." (Office Action, p. 8). However, regarding claim 8, Applicants submit that any proposed combination of the Hang reference and the Thome reference does not teach or suggest the claim limitations calling for "***at least one pointer register configured to maintain a previous read***

counter setting of the at least one read counter", as claimed by Applicants in independent claim 8 from which claim 9 through 10 depend. Therefore, Applicants respectfully request that the rejection to claims 8 through 10 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in View of U.S. Patent No. 5,426,612 to Ichige et al.

Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Ichige et al. (U.S. Patent No. 5,426,612). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 11 and 12 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Regarding independent claim 11, from which claim 12 depends, Applicants sustain the above-proffered arguments that Hang does not teach, disclose or motivate Applicants' invention as claimed. In contrast to the elements of the presently claimed invention of independent claim 11, nothing within the Hang reference discloses "***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter***", as uniquely taught by Applicants and claimed in independent claim 11.

The Office Action cites the Ichige reference for "teach[ing] that it was known in the art at the time the invention was made to incorporate a FIFO with associated pointer logic on a single semiconductor substrate/wafer. See figures 13-14, column 6 (lines 20-23), and column 22 (lines

37-45). (Office Action, p. 8). However, regarding claim 11, Applicants submit that any proposed combination of the Hang reference and the Ichige reference does not teach or suggest the claim limitations calling for "***at least one pointer register configured to maintain a previous read counter setting of the at least one read counter***", as claimed by Applicants in independent claim 11 from which claim 12 depends. Therefore, Applicants respectfully request that the rejection to claims 11 and 12 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in View of U.S. Patent No. 6,329,997 to Wu et al.

Claims 13 through 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Wu et al. (U.S. Patent No. 6,329,997). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 13 through 16 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Regarding independent claim 13, from which claims 14 through 16 depend, Applicants sustain the above-proffered arguments that Hang does not teach, disclose or motivate Applicants' invention as claimed. In contrast to the elements of the presently claimed invention of independent claim 13, nothing within the Hang reference discloses "***a read counter associated***

with the FIFO and configured to maintain a previous read counter setting of the read counter", as uniquely taught by Applicants and claimed in independent claim 13.

The Office Action cites the Wu reference for "teach[ing] that it was known to incorporate a FIFO on the same substrate with a DRAM. See column 3, lines 8-20). (Office Action, p. 9). However, regarding claim 13, Applicants submit that any proposed combination of the Hang reference and the Wu reference does not teach or suggest the claim limitations calling for "***a read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter***", as claimed by Applicants in amended independent claim 13 from which claims 14 through 16 depend. Therefore, Applicants respectfully request that the rejection to claims 13 through 16 be withdrawn.

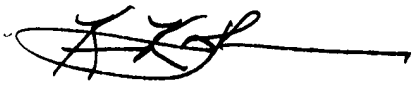
ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 13, 17, 23 and 25 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 25 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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